## Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

Claims 1-18 (Canceled)

Claim 19 (Previously Presented): A semiconductor intermediate product, comprising:

a semiconductor wafer having a plurality of device surface areas which are separated from one another by scribe lines, wherein each of the device surface areas includes a substrate mounting region and a plurality of surface electrodes adjacent the substrate mounting region;

a plurality of wiring substrates fixed to the substrate mounting region of the plurality of device surface areas, respectively, wherein a peripheral surface region of each of the wiring substrates includes a plurality of electrode pads;

a plurality of wiring bondings which connect the plurality of electrode pads to the plurality of surface electrodes within each of the plurality of device surface areas; and

a resin contained between adjacent wiring substrates so as to cover the scribe lines, the electrode pads, the wiring bonding, and the surface electrodes between the adjacent wiring substrates within the resin.

Claim 20 (Previously Presented): The semiconductor intermediate product of claim 19, further comprising an insulating adhesive which fixes wherein the plurality of wiring substrates to the substrate mounting region of the respective plurality of device surface areas.

Claim 21 (Previously Presented): The semiconductor intermediate product of claim 19, wherein the peripheral surface region of each of the wiring substrates is stepped down from a central surface region of each of the wiring substrates, and wherein the resin covers the peripheral surface region of each of the wiring substrates and does not cover the central surface region of each of the wiring substrates.

Claim 22 (Previously Presented): The semiconductor intermediate product of claim 20, wherein the peripheral surface region of each of the wiring substrates is stepped down from a central surface region of each of the wiring substrates, and wherein the resin covers the peripheral surface region of each of the wiring substrates and does not cover the central surface region of each of the wiring substrates.

Claim 23 (New): A semiconductor wafer product comprising:

a semiconductor wafer having a plurality of chip areas and a plurality of scribe areas that divide the chip areas, each of the chip areas having a central area at which

an integrated circuit is formed and an electrode area surrounding the central area, wherein a plurality of first electrode pads are formed in the electrode area;

a plurality of wiring substrates formed on the central areas, each of the wiring substrates having a plurality of external electrodes formed in a center area thereof and a plurality of second electrodes pads respectively electrically connected to the external electrodes, formed in a peripheral area thereof;

a plurality of bonding wires each of which respectively connects one of the first electrode pads with one of the second electrode pads; and

a resin formed on the electrode areas, the peripheral areas of the wiring substrates and the scribe areas, so that the resin covers the first and second electrode pads and the bonding wires.

Claim 24 (New): The semiconductor wafer product according to claim 23, wherein a plurality of scribe lines are formed on the scribe areas.

Claim 25 (New): The semiconductor wafer product according to claim 23, wherein each of the wiring substrates include a plurality of through holes formed therethrough, a conductive material formed in the through holes and a plurality of wirings electrically connected to the second electrode pads.

Claim 26 (New): The semiconductor wafer product according to claim 25, wherein each of the external electrodes are respectively electrically connected to the second electrode pads through the conductive material and the wirings.

Claim 27 (New): The semiconductor wafer product according to claim 23, wherein a top surface of the resin has substantially the same level as top surfaces of the wiring substrates.

Claim 28 (New): The semiconductor wafer product according to claim 23, wherein the external electrodes are formed in peripheral regions of the central areas of the wiring substrates.

Claim 29 (New): The semiconductor wafer product according to claim 23, wherein the external electrodes are ball electrodes.

Claim 30 (New): A semiconductor wafer product comprising:

a semiconductor wafer having a plurality of chip regions and scribe regions separating the chip regions, wherein each of the chip regions has a central region at which an integrated circuit is formed and a peripheral region at which a plurality of first electrode pads are formed;

a plurality of wiring substrates respectively formed on the central regions of the chip regions, wherein each of the wiring substrates has a plurality of external electrodes formed in a center area thereof and a plurality of second electrode pads respectively electrically connected to the external electrodes formed in a peripheral area thereof;

a plurality of bonding wires respectively connecting the first electrode pads with the second electrode pads; and

a resin material formed on the semiconductor wafer except for the center areas of the wiring substrates, so that the resin material covers the first and second electrode pads and the bonding wires.

Claim 31 (New): The semiconductor wafer product according to claim 30, wherein a plurality of scribe lines are formed in the scribe regions of the semiconductor wafer.

Claim 32 (New): The semiconductor wafer product according to claim 30, wherein each of the wiring substrates include a plurality of through holes formed therethrough, a conductive material formed in the through holes and a plurality of wirings respectively electrically connected to the second electrode pads.

Claim 33 (New): The semiconductor wafer product according to claim 32, wherein each

of the external electrodes are respectively electrically connected to the second electrode pads through the conductive material and the wirings.

Claim 34 (New): The semiconductor wafer product according to claim 30, wherein a top surface of the resin material has substantially a same level as top surfaces of the wiring substrates.

Claim 35 (New): The semiconductor wafer product according to claim 30, wherein the external electrodes are formed in peripheral regions of the center areas of the wiring substrates.

Claim 36 (New): The semiconductor wafer product according to claim 30, wherein the external electrodes are ball electrodes.